Toshiba Develops Time-Domain Analog and Digital Mixed-Signal Processing Circuitry

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- To reduce 38% of error correction circuit of NAND flash memory -

Toshiba Corporation (TOKYO:6502) today announced that it has developed time-domain analog and digital mixed-signal processing circuitry with the potential to replace general digital signal processing in error correction. The technology cuts the gate count of the low-density parity-check (LDPC) decoder used in error correction of NAND flash memory by 38% and will support Toshiba in enhancing cost competitiveness. The circuit was introduced at the International Solid-State Circuit Conference in San Francisco on February 20, 2013.

With advances in capacity, error correction is more important than ever in ensuring the reliability of NAND flash memories. Advanced error correction with improved correction rates is also a must in wireless communication. In both areas, LDPC code is one of the most promising error correction codes.

The problem with LDPC decoder circuitry is that it uses probability information in volumes that surpass that of the bit information utilized in classic error correction techniques, resulting in a large gate count. Efforts to overcome this include using an analog quantity, such as voltage, to represent probability information. This reduces the wiring required to represent information, as a single wire can contain multi-bit analog information but only one bit of digital information. However, this approach is impractical, as the large-scale system required cannot be designed with widely used design automation tools. There is also the problem of integrating analog-to-digital and digital-to-analog converters, which are large and power hungry.

Toshiba's time-domain analog and digital mixed-signal processing uses "time" to represent information. Like a voltage-based analog signal, "time" can contain multi-bit information, but its interface circuits, time-to-digital and digital-to-time converters, are smaller and consume less power than ADC and DAC. All the circuit elements are digital, allowing use of standard design automation tools, can be easily applied to large scale systems.

Toshiba has fabricated LDPC decoder and demonstrated that the gate count is 38% lower than with general digital implementation.

Mr. Daisuke Miyashita, a specialist of Toshiba Center for Semiconductor Research & Development who worked for the development said "We are going to advance research and development of the proposed method, with the objective of applying it to various systems, including LDPC decoders that handle large volumes of information."

Language:
English


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